

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT299

8-bit universal shift register; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

8-bit universal shift register; 3-state

74HC/HCT299

FEATURES

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes:
 - shift left
 - shift right
 - hold (store)
 - load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability: bus driver (parallel I/Os), standard (serial outputs)
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (S₀ and S₁), as shown in the mode select table.

All flip-flop outputs have 3-state buffers to separate these outputs (I/O₀ to I/O₇) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q₀ and Q₇) are used for expansion in serial shifting of longer words.

A LOW signal on the asynchronous master reset input ($\overline{\text{MR}}$) overrides the S_n and clock (CP) inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on the 3-state output enable inputs ($\overline{\text{OE}}_1$ or $\overline{\text{OE}}_2$) disables the 3-state buffers and the I/O_n outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S₀ and S₁, when in preparation for a parallel load operation.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay CP to Q ₀ , Q ₇ CP to I/O _n	C _L = 15 pF; V _{CC} = 5 V	20	19	ns
t _{PHL}	$\overline{\text{MR}}$ to Q ₀ , Q ₇ or I/O _n		20	19	ns
f _{max}	maximum clock frequency		20	23	ns
C _I	input capacitance		50	46	MHz
C _{I/O}	input/output capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	10	10	pF
			120	125	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

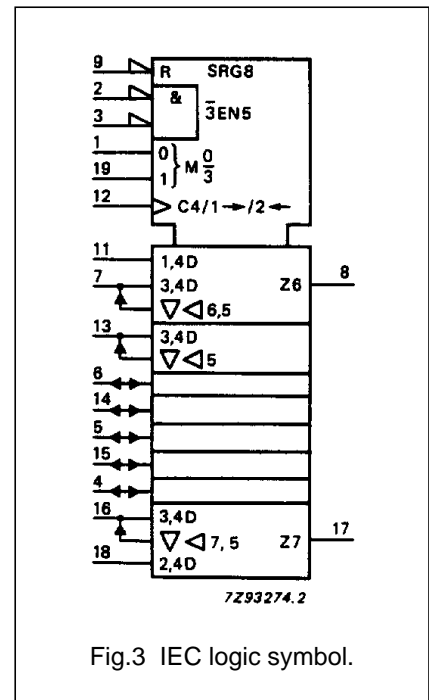
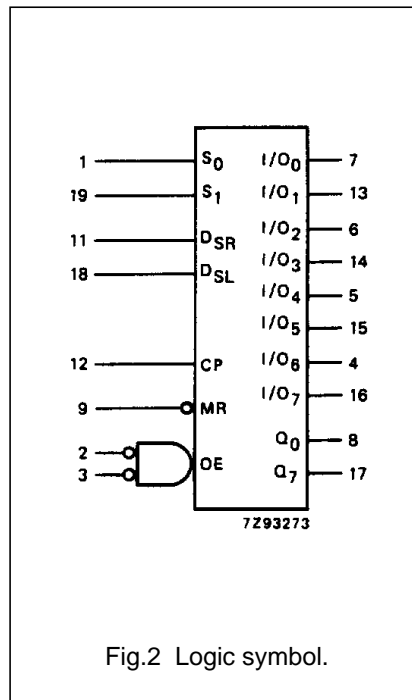
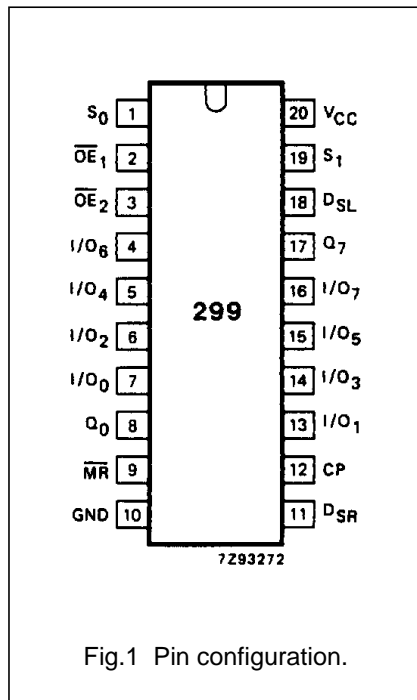
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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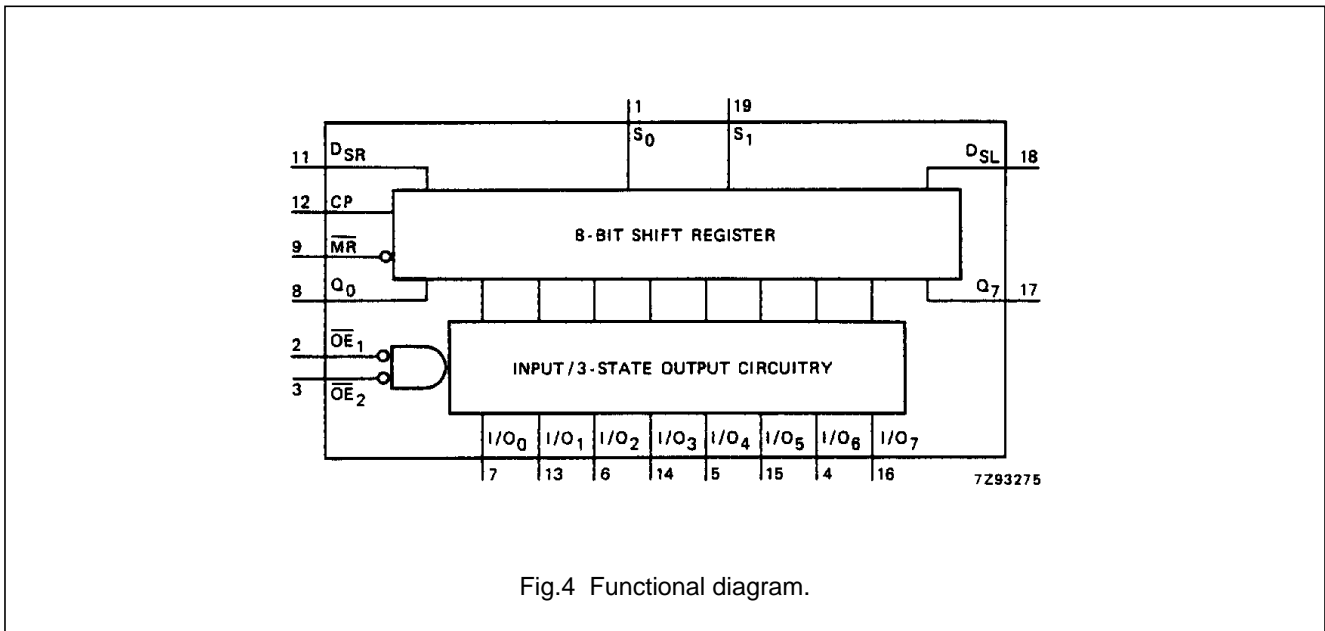
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	S_0, S_1	mode select inputs
2, 3	$\overline{OE}_1, \overline{OE}_2$	3-state output enable inputs (active LOW)
7, 13, 6, 14, 5, 15, 4, 16	I/O ₀ to I/O ₇	parallel data inputs or 3-state parallel outputs (bus driver)
8, 17	Q ₀ , Q ₇	serial outputs (standard output)
9	\overline{MR}	asynchronous master reset input (active LOW)
10	GND	ground (0 V)
11	D _{SR}	serial data shift-right input
12	CP	clock input (LOW-to-HIGH, edge-triggered)
18	D _{SL}	serial data shift-left input
20	V _{CC}	positive supply voltage



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MODE SELECT TABLE

INPUTS				RESPONSE
\overline{MR}	S_1	S_0	CP	
L	X	X	X	asynchronous reset; $Q_0-Q_7 = \text{LOW}$
H	H	H	\uparrow	parallel load; $I/O_n \rightarrow Q_n$
H	L	H	\uparrow	shift right; $D_{SR} \rightarrow Q_0, Q_0 \rightarrow Q_1$ etc.
H	H	L	\uparrow	shift left; $D_{SL} \rightarrow Q_7, Q_7 \rightarrow Q_6$ etc.
H	L	L	X	hold

Notes

- H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 \uparrow = LOW-to-HIGH CP transition

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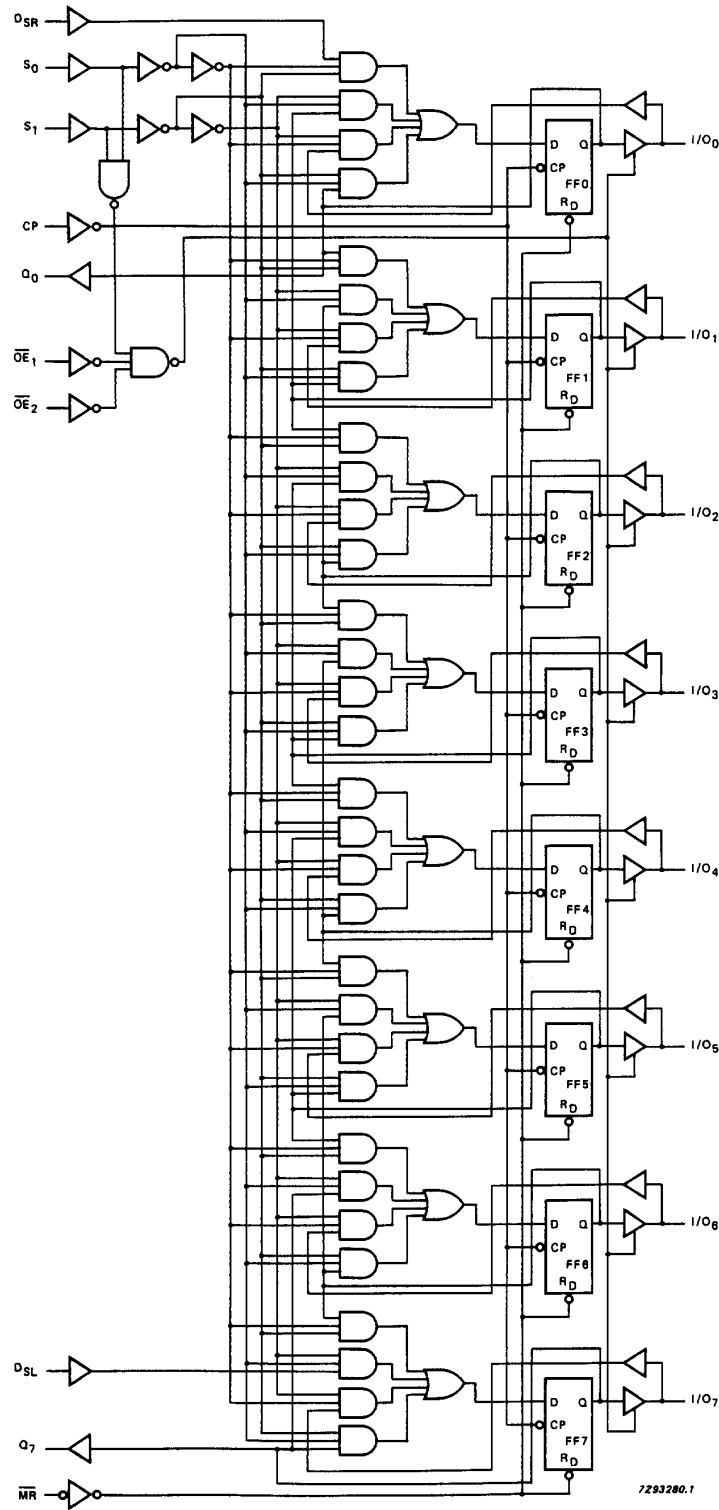


Fig.5 Logic diagram.

8-bit universal shift register; 3-state

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver (parallel I/Os)
standard (serial outputs)

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q ₀ , Q ₇		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay CP to I/O _n		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6
t _{PHL}	propagation delay MR to Q ₀ , Q ₇ or I/O _n		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.7
t _{PZH}	3-state output enable time \overline{OE}_n to I/O _n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9
t _{PZL}	3-state output enable time \overline{OE}_n to I/O _n		41 15 12	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig.9
t _{PHZ}	3-state output disable time \overline{OE}_n to I/O _n		66 24 19	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.9
t _{PLZ}	3-state output disable time \overline{OE}_n to I/O _n		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9
t _{THL} / t _{TLH}	output transition time bus driver (I/O _n)		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time standard (Q ₀ , Q ₇)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t _w	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t _w	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7

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SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{rem}	removal time MR to CP	5	-14		5		5		ns	2.0	Fig.7
		5	-5		5		5			4.5	
		5	-4		5		5			6.0	
t _{su}	set-up time D _{SR} , D _{SL} to CP	100	33		125		150		ns	2.0	Fig.6
		20	12		25		30			4.5	
		17	10		21		26			6.0	
t _{su}	set-up time S ₀ , S ₁ to CP	100	33		125		150		ns	2.0	Fig.8
		20	12		25		30			4.5	
		17	10		21		26			6.0	
t _{su}	set-up time I/O _n to CP	125	39		155		190		ns	2.0	Fig.6
		25	14		31		38			4.5	
		21	11		26		32			6.0	
t _h	hold time I/O _n , D _{SR} , D _{SL} to CP	0	-14		0		0		ns	2.0	Fig.6
		0	-5		0		0			4.5	
		0	-4		0		0			6.0	
t _h	hold time S ₀ , S ₁ to CP	0	-28		0		0		ns	2.0	Fig.8
		0	-10		0		0			4.5	
		0	-8		0		0			6.0	
f _{max}	maximum clock pulse frequency	5.0	15		4.0		3.4		MHz	2.0	Fig.6
		25	45		20		17			4.5	
		29	54		24		20			6.0	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver (parallel I/Os)
standard (serial outputs)

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I/O _n	0.25
D _{SR} , D _{SL}	0.25
CP, S ₀	0.60
\overline{MR} , S ₁	0.25
\overline{OE}_n	0.30

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AC CHARACTERISTICS FOR 74HCT

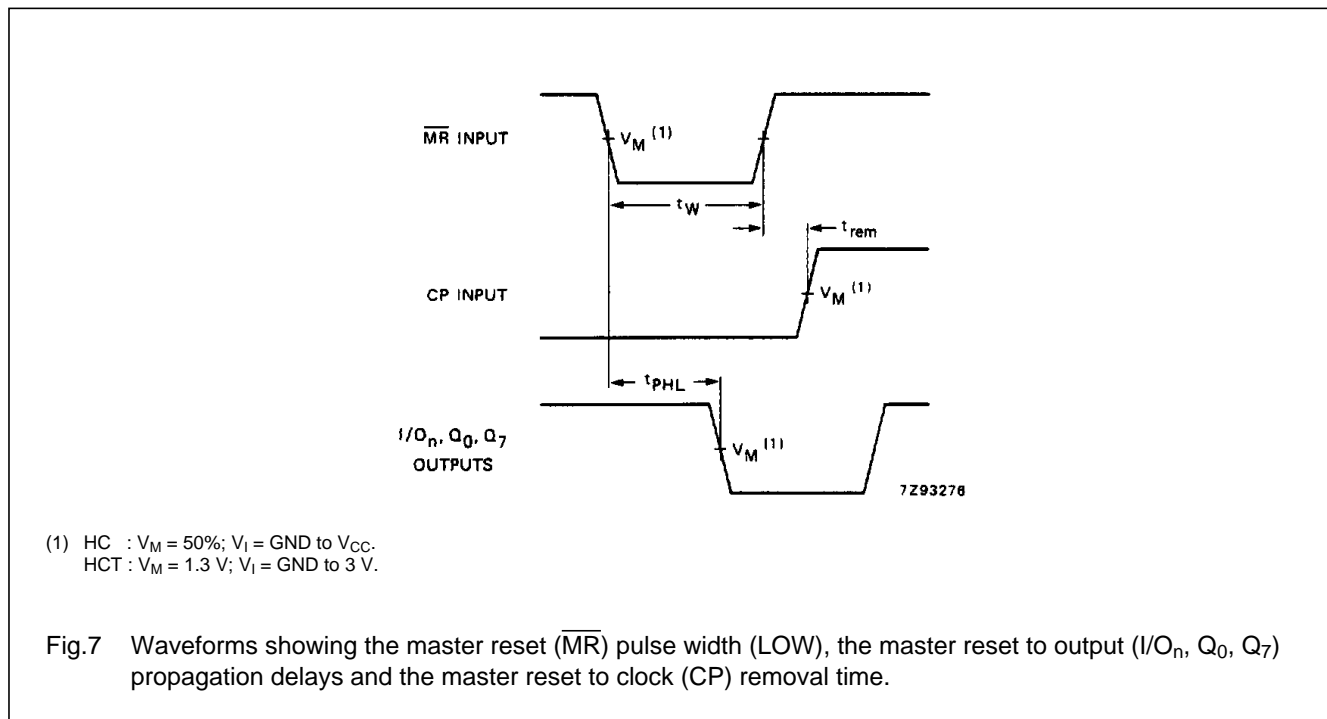
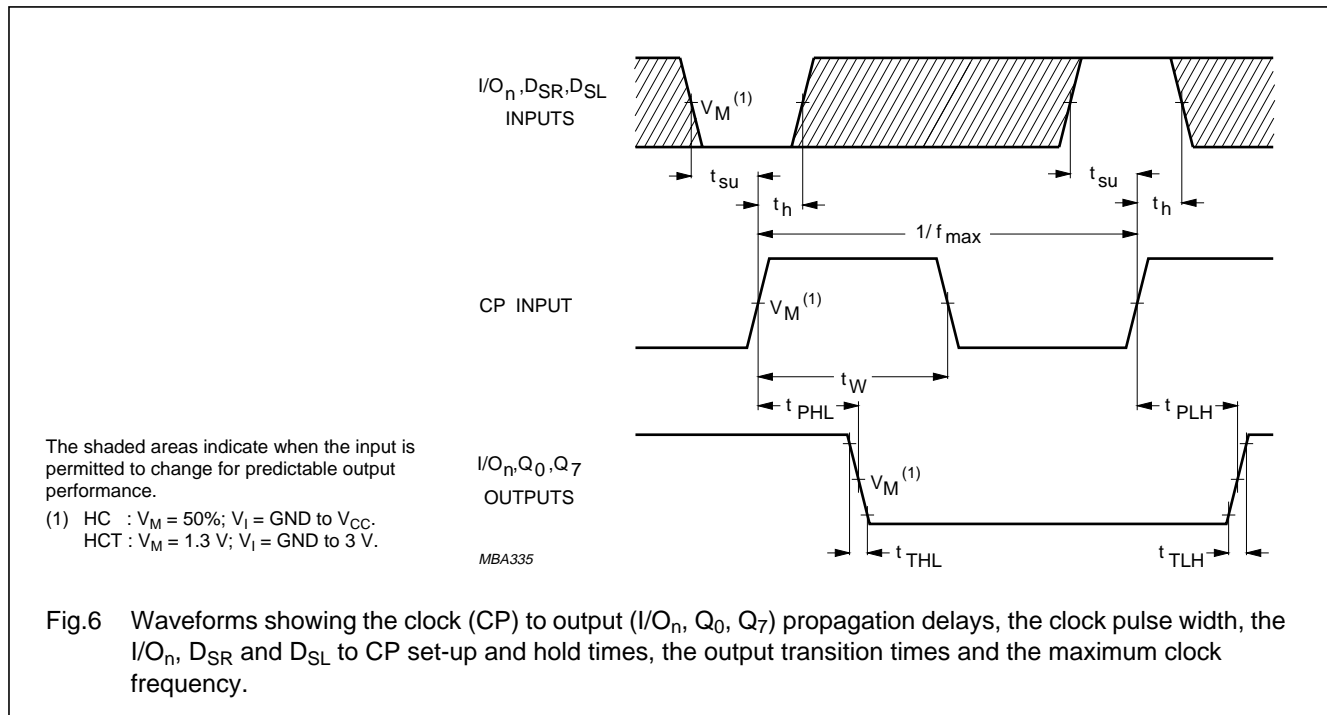
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V_{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t_{PHL}/t_{PLH}	propagation delay CP to Q_0, Q_7		22	37		46		56	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP to I/O_n		22	37		46		56	ns	4.5	Fig.6
t_{PHL}	propagation delay \overline{MR} to Q_0, Q_7 or I/O_n		27	46		58		69	ns	4.5	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE}_n to I/O_n		19	30		38		45	ns	4.5	Fig.9
t_{PHZ}	3-state output disable time \overline{OE}_n to I/O_n		24	37		46		56	ns	4.5	Fig.9
t_{PLZ}	3-state output disable time \overline{OE}_n to I/O_n		20	32		40		48	ns	4.5	Fig.9
t_{THL}/t_{TLH}	output transition time bus driver (I/O_n)		5	12		15		18	ns	4.5	Fig.6
t_{THL}/t_{TLH}	output transition time standard (Q_0, Q_7)		7	15		19		22	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	20	10		25		30		ns	4.5	Fig.6
t_W	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig.7
t_{rem}	removal time MR to CP	10	2		9		11		ns	4.5	Fig.7
t_{su}	set-up time $I/O_n, D_{SR}, D_{SL}$ to CP	25	14		31		38		ns	4.5	Fig.6
t_{su}	set-up time S_0, S_1 to CP	32	18		40		48		ns	4.5	Fig.8
t_h	hold time $I/O_n, D_{SR}, D_{SL}$ to CP	0	-11		0		0		ns	4.5	Fig.6
t_h	hold time S_0, S_1 to CP	0	-17		0		0		ns	4.5	Fig.8
f_{max}	maximum clock pulse frequency	25	42		20		17		MHz	4.5	Fig.6

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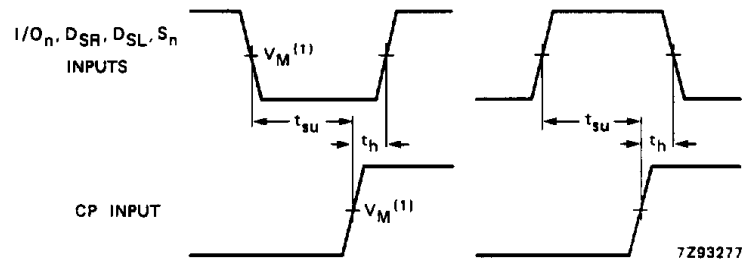
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AC WAVEFORMS



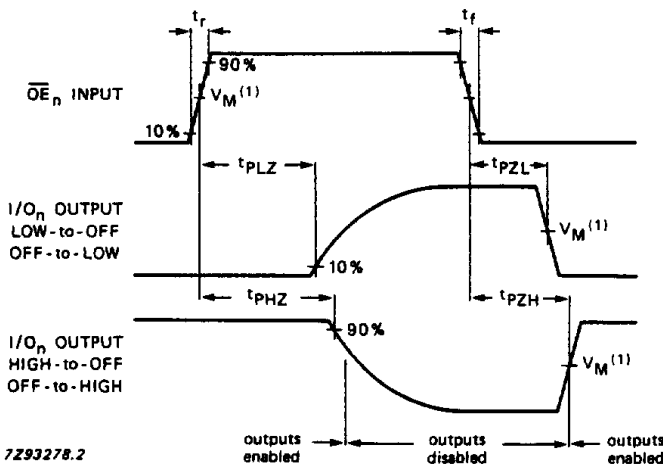
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(1) HC : V_M = 50%; V_I = GND to V_{CC}.
 HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the set-up and hold times from the mode control inputs (S₀, S₁) to the clock (CP).



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
 HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the 3-state enable and disable times for OE_n inputs.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".